REMARKS

Reconsideration and allowance are respectfully requested.

The claims are amended to replace "operable" with "configured." Dependent claims 3, 14, and 31 are amended to recite that the anticipated timing information includes timing values indicative of a speculative time during which that data transfer is predicted will occur over the bus. Example support is found at page 9, line 2-page 10, line 5. As explained at page 2, lines 16-23 and page 3, lines 1-4, the anticipated timing information is based on a probability/assumption that may not prove to be accurate. Hence, the anticipated timing is speculative and a prediction.

Claims 1-46 stand rejected under 35 U.S.C. §103 as being obvious based on Fischer, Thekkath, and newly-cited Best. The Examiner appears to be using Best to teach multiple bus masters and multiple bus slaves. This rejection is respectfully traversed.

Fischer describes an asynchronous network that adjusts the timing of data transmission so as to adapt to the network load. This adjustment takes place for future transactions based upon the result of preceding transactions. The Examiner admits that Fischer does not simulate the master-slave transaction or compensate for two or more concurrent transactions.

Thekkath discloses a system with a bus arbiter. The Examiner suggests that Thekkath discloses simulating the bus/master device referring to col. 6, line 57-col. 7, line 5. Nothing in this text says anything about simulation. The text at col. 5, lines 29-31 does not teach simulation, rather it teaches providing design information in a machine-readable form describing the hardware design of Thekkath which could then be subject to simulation by some other system. But Thekkath itself gives no information as to how this simulation is actually performed. Certainly, this general statement in Thekkath fails to teach the specific simulation

steps recited in claim 1. Thus, the Examiner's statement that Thekkath "meets the claim" because Thekkath's general statement of intended use is simply not accurate.

Nor does Thekkath describe generating anticipated timing data by assuming that the data transfer will occur with exclusive access to the bus. The Examiner cites [0012] of Fischer for this feature. But there is no teaching in [0012] where it is assumed that data transfer will occur with exclusive access to the bus. Fischer may determine timing information, but this is not timing information based upon a specified assumption of exclusive bus access as specified in the claims. Indeed, the bus arbiter in Thekkath ensures that each bus transaction in Thekkath will have exclusive access to the bus. As a result, there is no need in Thekkath for anticipated timing information or any assumption that data transfers will occur with exclusive access to the bus. Nor does Thekkath teach the generation of timing information whether anticipated based upon an assumption or otherwise. Thus, neither Fischer nor Thekkath discloses generating anticipated timing information by assuming that the data transfer will occur with exclusive access to the bus.

Thekkath does not disclose determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus. Fischer operates at a much higher statistical level than individual data bus transfers. The Examiner cites col. 5, lines 1-10 of Thekkath as disclosing "detecting what would be the capability of the bus." But these lines do not disclose detecting a bus capability; instead, they state that the "slave configuration logic stores a burst transaction capability corresponding to the slave device." The burst transaction capability is a capability of the slave device—not the bus. Column 5, lines 6-7 confirms this: "By configuring bursts sequences in accordance with the slave device's ability to accept bursts...." So Thekkath does not detect a capability of the bus.

But even if Thekkath did disclose detecting a capability of the bus, (which it does not), that would not disclose "determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus." Detecting a capability of the bus is not the same as determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus. Thekkath describes bus arbitration logic 104 at col. 7, lines 1-31 as simply determining whether transaction requests have been received from initiating devices, and granting or refusing requests according to an arbitration algorithm. There is no description of analyzing any anticipated timing information associated with the requests to determine whether two or more concurrent data transfers would occur on the bus.

Because Thekkath is a system in which concurrent data transfers are prevented by the action of the bus arbiter, Thekkath never gets as far as generating anticipated timing information that would indicate concurrent data transfers. In fact, Thekkath precludes this possibility from ever arising.

Simulating Thekkath with its precise bus arbitration would incur the complexity and decreased speed of simulation which the claimed technology seeks to avoid. The inventors in this application recognized that bus contention is, in practice, relatively rare, and so it is more efficient to generate anticipated timing information and then check this for overlap with an appropriate correction as necessary rather than simulating the behavior of the bus arbitration mechanism. This is permissible in the simulation environment as it is possible to rerun the activity using bus status information to correct the anticipated timing information. In a real hardware system such as Thekkath's, if bus contention is allowed to occur, it is already too late, and incorrect or unpredictable operation is likely to result.

Fischer and Thekkath do not disclose generating machine-readable revised timing information for those data transfers. The Examiner states that "Fischer teaches that continuous revisions take place to adjust for the transaction interference, or errors, of Thekkath in paragraph 0012 [of Fischer], "Each slave node clock is continuously corrected compared with the master node clock to smooth slave clock error to an average of zero compared with the master clock...." However, the continuous slave node clock correction of Fischer is not a correction of timing information. The slave node clock is a clock signal that controls operation of the slave device. The slave node clock is not timing information for concurrent data transfers, as recited in the claims. Fischer does not describe revising anticipated timing information for two or more concurrent data transfers because Fischer's clock correction is at a much higher statistical level than at the individual bus conflict level. Furthermore, the correction in Fischer is effectively a feedback system that uses an error in the detected clock to correct future behavior concerning different future transactions rather than the ones which actually gave rise to the error concerned. While this behavior might be acceptable in Fischer's system, it would not be acceptable when simulating the operation of a data processing apparatus as the data processing apparatus would be simulated with the incorrect behavior and problems due to bus conflicts would not be properly modeled.

The Examiner also argues that Thekkath is being used for the teaching of concurrent data transfers. But the Examiner previously emphasized that concurrent data transfers do not actually occur in Thekkath. There is no disclosure or suggestion in either Fischer or Thekkath of generating machine-readable revised timing information for the concurrent data transfers for use in correcting the previously-generated anticipated timing information.

Notwithstanding the Examiner's contentions otherwise, Applicants maintain that Fischer and Thekkath are in different arts. Thekkath is in the field of computer system bus architectures (col. 1, lines 25-26) and teaches a computer system comprising a system bus and various processing circuits connected to the bus (see Figure 1). Each processing circuit is housed in a common computer housing. The various processing circuits 104-120 operate under control of the central processing unit 102. In contrast, Fischer is in the field of communications networks. The "nodes" of the network in Fischer are separate devices within a communications network, such as computers, printers, scanners, telephones, televisions, cameras etc (see [0106] and Figures 1a-1c of Fischer). There is no one central processing unit that operates the various devices in the network—each device has its own control capability.

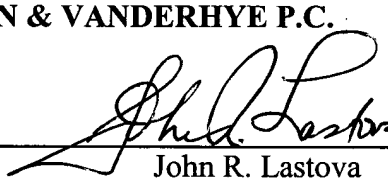
There is no reasonable basis for a skilled person to use a technique for arbitrating requests for transfers on an internal system bus in communications between separate nodes externally connected by a network. Fischer's communications network will typically have many thousands of terminals (see the many houses in Figure 1c of Fischer) with fiber optic cables being used so that multiple data transfers can be carried across the network at the same time. The Examiner admits that Fischer does not compensate for two or more concurrent transactions. The reason Fischer does not do such compensation is that preventing two or more concurrent transactions would result in thousands of people being cut off from the network every time a single person uses the network, which would not be sensible. Given that this kind of exclusive access to the network is clearly undesirable in a network such as Fischer's, the skilled person would not introduce a bus arbiter (as described in Thekkath) into the network in order to enforce exclusive network access.

The Examiner argues the combination "because it is desirable to test and simulate for 'a burst data transaction to be optimized ...for efficient transfer over a bus'" and because having two devices transfer data on the bus at the same time precludes any transfer of data. Following the Examiner's motivation in this case, the bus arbiter of Thekkath would be modeled so that bus contention is prevented from ever occurring at the expense of a slower and more complex simulation. Thus, the combination suggested by the Examiner is one in which there would be no generation of anticipated timing information or correction of that anticipated timing information because with the Examiner's combination the modeled bus arbiter ensures that no correction is necessary. But that combination is not what is claimed.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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